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| **22bec121** |  |
| **Experiment – 5** | **Date:-15/2/2024** |

**Lab Work**

**Q1 .Post Lab Exercises**

# Code (Generated)

module snehexp5(

Mode,

CLK,

HIGH,

Q3,

Q2,

Q1,

Q0

);

input wire Mode;

input wire CLK;

input wire HIGH;

output reg Q3;

output wire Q2;

output wire Q1;

output wire Q0;

wire SYNTHESIZED\_WIRE\_0;

wire SYNTHESIZED\_WIRE\_1;

wire SYNTHESIZED\_WIRE\_2;

reg JKFF\_A;

reg JKFF\_2;

reg JKFF\_3;

assign Q2 = JKFF\_3;

assign Q1 = JKFF\_2;

assign Q0 = JKFF\_A;

always@(posedge SYNTHESIZED\_WIRE\_0)

begin

JKFF\_2 <= ~JKFF\_2 & HIGH | JKFF\_2 & ~HIGH;

end

always@(posedge SYNTHESIZED\_WIRE\_1)

begin

JKFF\_3 <= ~JKFF\_3 & HIGH | JKFF\_3 & ~HIGH;

end

always@(posedge SYNTHESIZED\_WIRE\_2)

begin

Q3 <= ~Q3 & HIGH | Q3 & ~HIGH;

end

always@(posedge CLK)

begin

JKFF\_A <= ~JKFF\_A & HIGH | JKFF\_A & ~HIGH;

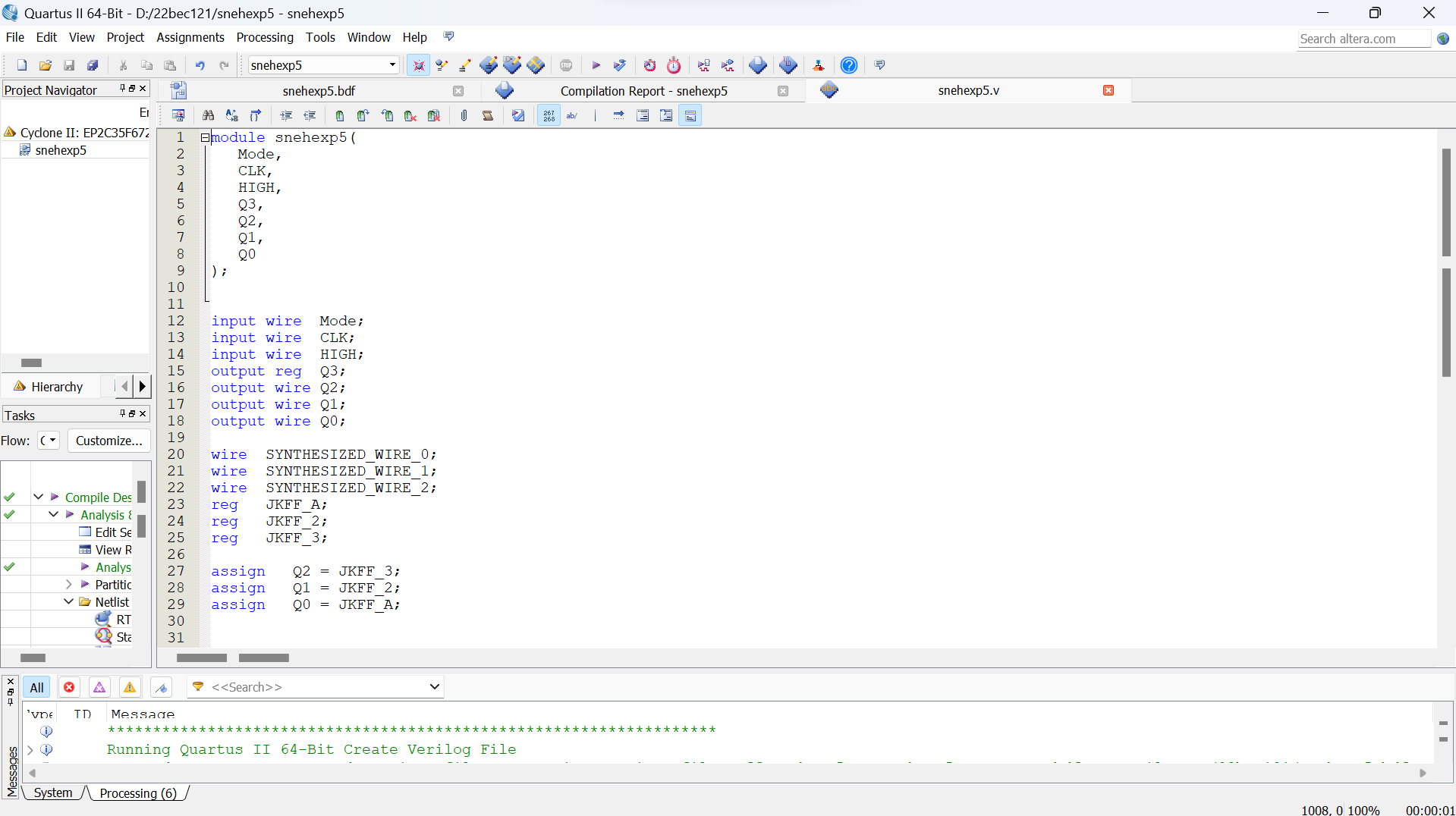
end

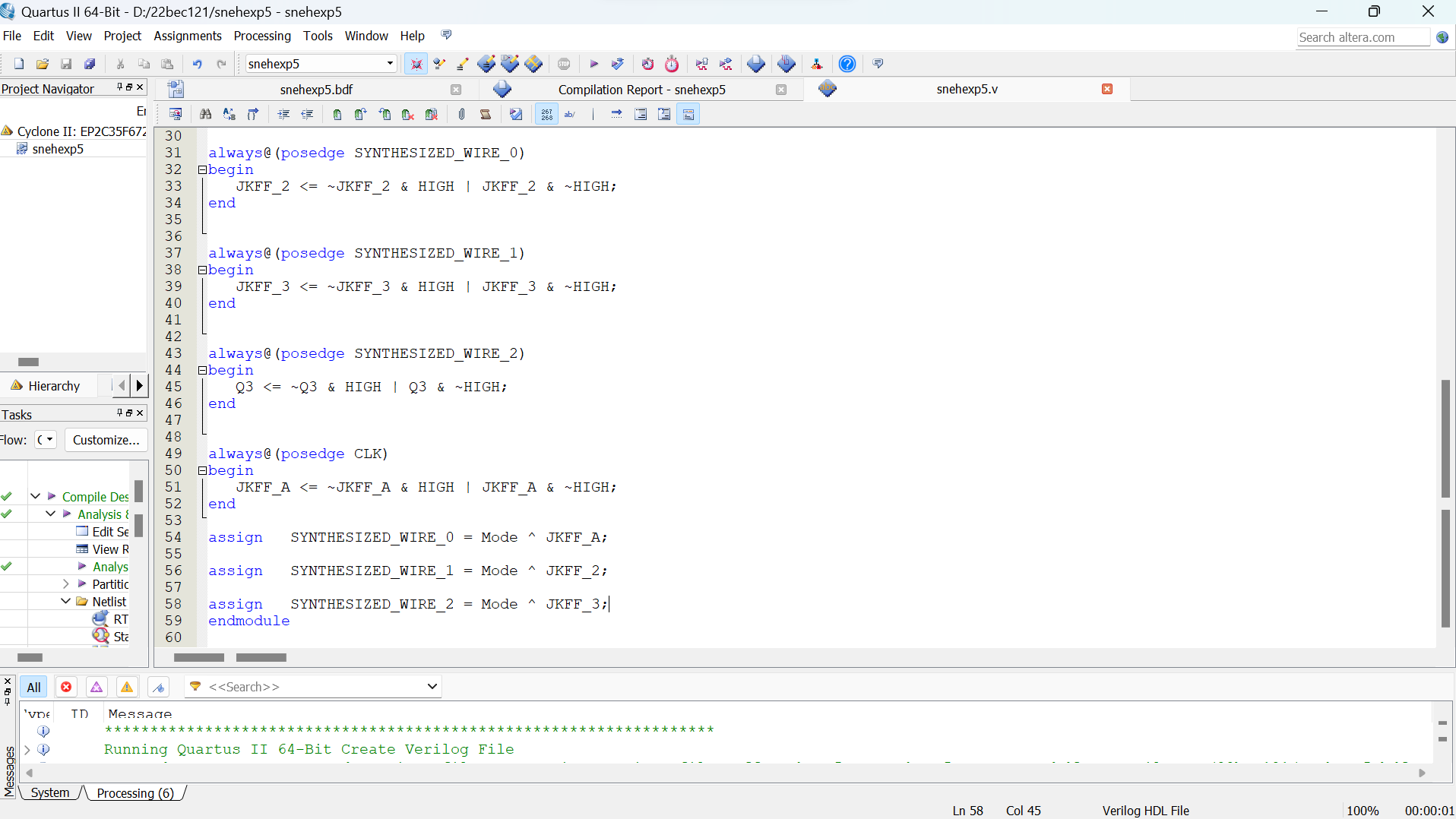
assign SYNTHESIZED\_WIRE\_0 = Mode ^ JKFF\_A;

assign SYNTHESIZED\_WIRE\_1 = Mode ^ JKFF\_2;

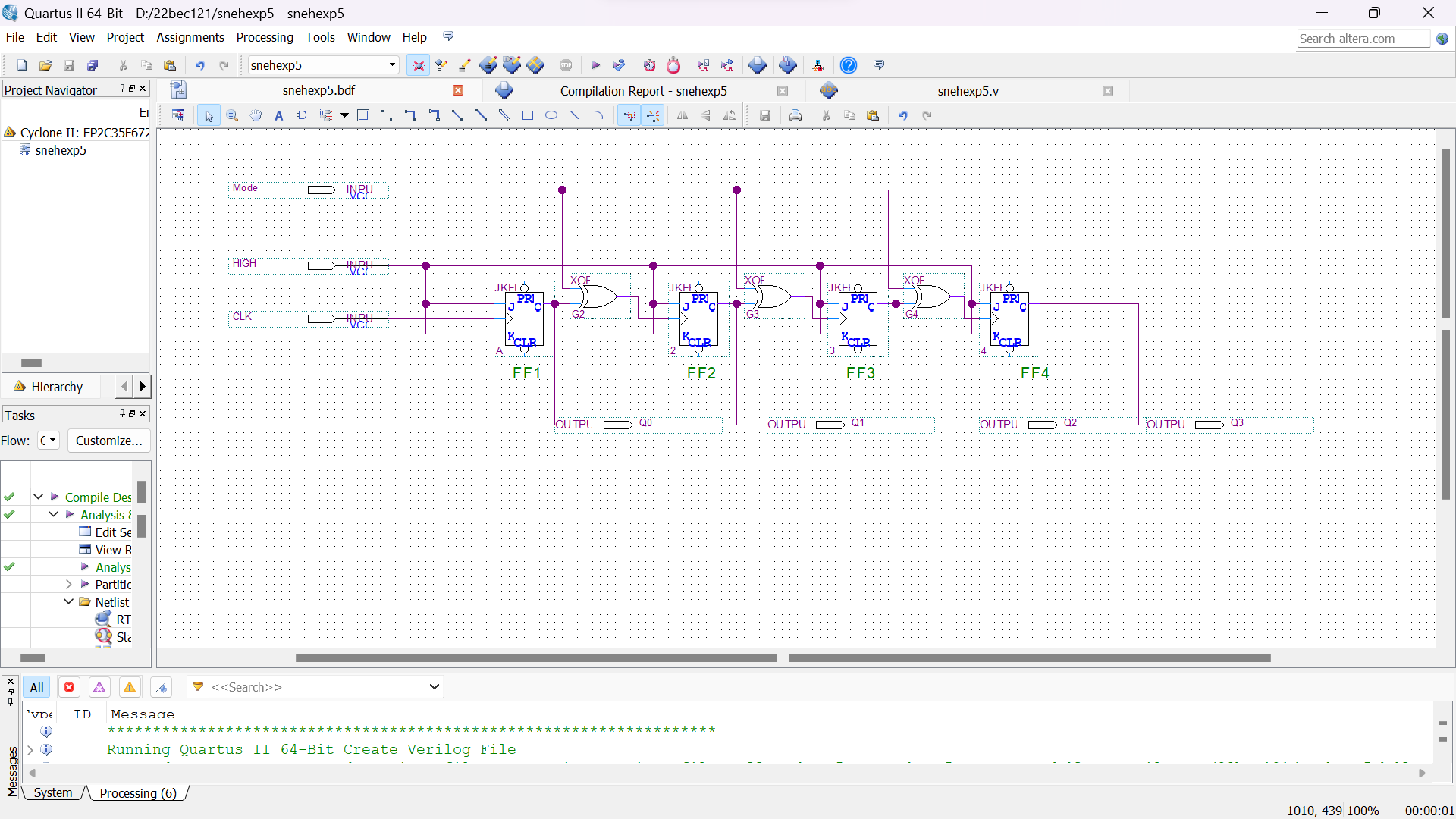
assign SYNTHESIZED\_WIRE\_2 = Mode ^ JKFF\_3;

endmodule

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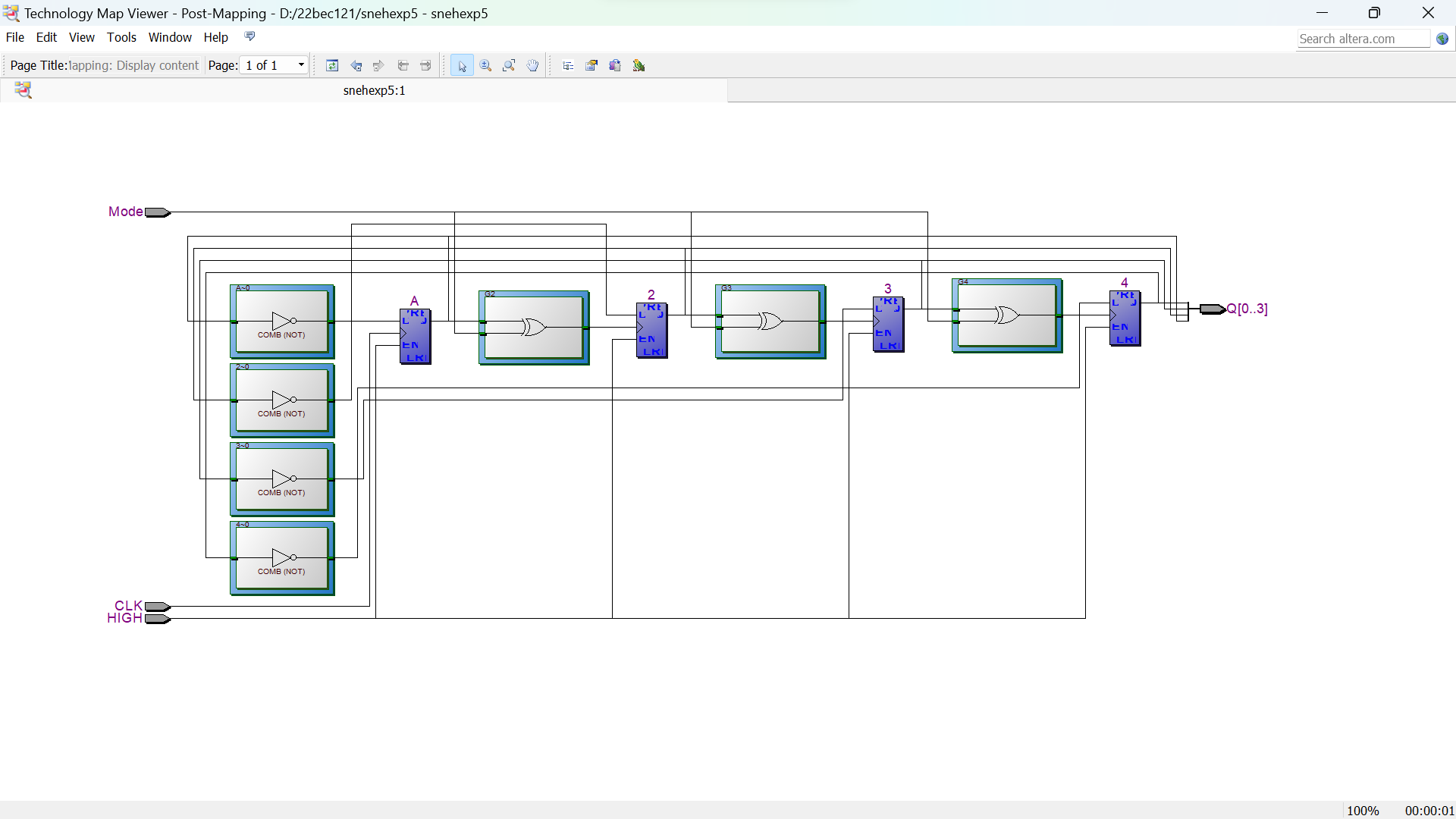
**Block Design**

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# Output 1)Cyclone II (RTL View)

# 

**2)Cyclone II (TTL View)**

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**Conclusion :- In this experiment we learnt that how we can implement any circuit using Block Diagrams .**

**This is a tedious way to implement a circuit but it is a way to develop small circuits with ease .**

**We also generated Verilog Code from the Block Diagram to implement a 4 bit Up/Dow Counter .**